Using Continuization in Reachability Analysis for the Verification of a Phase-Locked Loop

Matthias Althoff* Akshay Rajhans* Bruce H. Krogh* Soner Yaldiz* Xin Li* Larry Pileggi*

* Department of Electrical and Computer Engineering Carnegie Mellon University, 5000 Forbes Ave., Pittsburgh, PA 15213 Email: {malthoff|krogh|arajhans|syaldiz|xinli|pileggi}@ece.cmu.edu

Preference for oral or poster presentation: The authors prefer an oral presentation, but would also accept a poster presentation.

Extended Abstract

Verifying that phase-locked loops (PLLs) will lock in an acceptable time for the entire range of initial states and process variations currently requires time-consuming Monte Carlo simulations [Kuo et al. (2009)]. The size and complexity of PLL circuits make verification of locking a challenging application for reachability analysis, which is often touted as an alternative to numerical simulation. Convergence to locking can take hundreds or even a few thousand cycles, which far exceeds the capabilities of typical reachability methods to compute overapproximations that are tight enough to prove anything useful, even for grossly simplified models of the PLL dynamics. This abstract present a new method for reachability analysis that overcomes these difficulties and achieves verification of PLL locking behavior with computation times comparable to, or better than, the time required for Monte Carlo simulation.

The proposed approach to reachability analysis leverages a recently developed method for computing reachable sets for linear and hybrid dynamic systems with uncertain inputs and uncertain parameters [Althoff et al. (2011a)]. This makes it possible to verify PLL locking using a behavioral model, where bounded input and parameter uncertainties represent the range of dynamic behaviors of the underlying circuits. If the range of behaviors represented by the behavioral model with bounded uncertainties includes all possible behaviors of the more detailed circuit models, proof of locking for the behavioral model implies locking for the full circuit model, including ranges of initial states and process variations. We note that simulation studies are needed to validate the behavioral model, but model validation can be carried out on parts of the overall PLL circuit rather than on the complete circuit.

The PLL behavioral model, shown in Fig. 1, is a hybrid dynamic system, due to the switching behavior of the phase frequency detector (PFD). The slow convergence to locking presents an insurmountable challenge for bruteforce reachability analysis because of the inevitable overapproximations that occur when reachable sets are propagated from one continuous mode to the next at each discrete switching instant [Althoff et al. (2010); Girard and Le Guernic (2008); Ramdani and Nedialkov (2009)]. We introduce two innovations to circumvent this problem. First, because of the linear nature of the RC circuit that computes the input to the VCO (basically PI gains), it is possible to use a discrete-time formulation that eliminates explicit computation of the continuous-time reachable sets. The discrete-time linear models are of the form: $x_{k+1} \in$ $\mathcal{A}x_k \oplus \mathcal{U}_k$, where $\mathcal{A} = [\underline{A}, \overline{A}]$ is an interval matrix, \mathcal{U}_k is a zonotope (special case of a polytope), $k \in \mathbb{N}$ is the cycle number, and the operation $C \oplus D = \{c + d | c \in C, d \in D\}$ is Minkowski addition. In this discrete-time model, the reachable sets for the continuous state variables (capacitor voltages, phase of the VCO output) are computed at each cycle of the reference input, using different input values and parameter values to capture appropriately the effects of the charge pumps for each dynamic mode. Parameter uncertainties capture the effects of timing variations in the PFD as well as the underlying process variations. Symmetry is also exploited. More details on these procedures will be described in [Althoff et al. (2011b)].

The second innovation, which is the focus of this paper, is to represent the propagation of reachable sets across the discrete switching times using appropriate bounds on parameters in the discrete-time linear models. This approach to eliminating hybrid dynamic switching, which we call continuization [Althoff et al. (2011a)], eliminates the overly conservative overapproximations that occur in traditional methods for computing reachable sets for hybrid systems. These overapproximations occur when the reachable set at some instant has a non-empty intersection with the guard condition for a discrete transition. To propagate the reachable states using the new continuous dynamics, this intersection needs to be overapproximated with a set within the class of representations being used by the method. In our case, this means that a zonotope needs to be constructed that contains the intersection. Continuization avoids the construction by instead introducing uncertain linear dynamics that cover the behaviors on both sides of the guard condition. Reachability continues with these dynamics until the reachable set has passed completely into the guard region for the transition, at which point the dynamics in the new mode can be used exclusively.

Table 1. Required cycles to lock.

initial	Reachability Analysis		Simulink	
phase	cycles to	cycles	(avg.) cycles	
difference	guarantee	to reach	to reach	
$\Delta \Phi(0)$	locking	\mathcal{I}_{start}	\mathcal{I}_{start}	
$[-1.0, -0.8]\pi$	2039	1845	1208.5	
$[-0.8, -0.6]\pi$	1981	1787	1161.1	
$[-0.6, -0.4]\pi$	1908	1714	1096.2	
$[-0.4, -0.2]\pi$	1811	1616	988.57	
$[-0.2, -0.0]\pi$	1652	1457	839.37	

Continuization is most effective when the dynamics in the adjacent modes are not extremely different. For the behavioral model of the PLL, continuization is applied to represent the propagation of the reachable sets each time the PFD switches the states of the charge pumps. This application fits well with the conditions for which continuization is effective. As an illustration of the results, Fig. 2 shows the reachable set and some simulation runs projected onto state variables v_i , v_{p1} in Fig. 1) for the first 200 cycles for a particular PLL starting with the initial phase difference $[-\pi, -0.8\pi]$.

Using the approach described above to compute reachable sets for the PLL behavioral model, verification of PLL locking is done in two steps. First, the transient behavior from the initial state to the locking condition is computed. We denote this set of states at which the system first enters the locking constraints by \mathcal{I}_{start} . Then, a second reachable state computation is applied to demonstrate that the set \mathcal{I}_{start} is invariant, which means the PLL is locked indefinitely. When locking is demonstrated, the proposed reachability method provides a bound on the number of cycles needed to lock.

For a particular PLL, the first column in Table 1 shows the number of cycles needed to lock for various sets of initial phase differences $\Delta \Phi(0)$. These numbers include the additional cycles required to show that the set \mathcal{I}_{start} is an invariant. The number of cycles to enter \mathcal{I}_{start} the first time is shown in the next column. These numbers are compared to the case when the system behavior is analyzed by a Monte Carlo simulation. Since the cycle number depends on the initial condition, the averages are listed. Note that the bound on the cycles to locking computed by reachability is not overly conservative.

Table 2 shows the time required to demonstrate locking for each of the ranges of initial conditions. This is compared to the time required to perform one MATLAB Simulink run of the hybrid system model which is particularly slow because of the need to detect the zero crossings in the PFD switching logic. Circuit simulators would be considerably faster than the MATLAB Simulink simulation. Nevertheless, these computation times demonstrate that the computation time for the proposed reachability analysis is likely to be competitive with the time to carry out full Monte Carlo analysis.

REFERENCES

M. Althoff, O. Stursberg, and M. Buss. Computing reachable sets of hybrid systems using a combination of zonotopes and polytopes. *Nonlinear Analysis: Hybrid Systems*, 4(2):233–249, 2010.

Table 2. Computation times.

init. phase	Reachability Analysis		Simulink (avg.)			
$\Delta \Phi(0)$	total $[s]$	1 cycle [s]	total $[s]$	1 cycle [s]		
$[-1.0, -0.8]\pi$	55.0461	0.0270	48.3297	0.0237		
$[-0.8, -0.6]\pi$	54.4418	0.0275	47.9096	0.0242		
$[-0.6, -0.4]\pi$	53.4820	0.0280	46.2673	0.0242		
$[-0.4, -0.2]\pi$	47.8208	0.0264	44.4596	0.0245		
$[-0.2, -0.0]\pi$	42.9191	0.0260	38.5102	0.0233		
$\Phi_{ref} phase UP \qquad $						



Fig. 1. Phase-locked loop.



- Fig. 2. Reachable sets of each cycle for the first 200 cycles. Simulation results of each cycle are plotted by dots.
- M. Althoff, C. Le Guernic, and B. H. Krogh. Reachable set computation for uncertain time-varying linear systems. In *Hybrid Systems: Computation and Control*, 2011a.
- M. Althoff, A. Rajhans, B. H. Krogh, S. Yaldiz, X. Li, and L. Pileggi. Formal verification of digital phase-locked loops using reachability analysis. In *in preparation*, 2011b.
- A. Girard and C. Le Guernic. Zonotope/hyperplane intersection for hybrid systems reachability analysis. In Proc. of Hybrid Systems: Computation and Control, LNCS 4981, pages 215–228. Springer, 2008.
- C.-C. Kuo, M.-J. Lee, C.-N. Liu, and C.-J. Huang. Fast statistical analysis of process variation effects using accurate PLL behavioral models. *IEEE Transactions* on Circuits and Systems, 56(6):1160–1172, 2009.
- N. Ramdani and N. S. Nedialkov. Computing reachable sets for uncertain nonlinear hybrid systems using interval constraint propagation techniques. In Proc. of the 3rd IFAC Conference on Analysis and Design of Hybrid Systems, pages 156–161, 2009.